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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#15/Appeal Brief
7/10/01
V. Vannall

In re application of

THEODORE W. HOUSTON

Serial No. 09/346,436 (TI-21004)

Filed July 1, 1999

For: BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER

Art Unit 2813

Examiner E. Kielin

Commissioner for Patents
Washington, D. C. 20231

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 4, 7 to 9 and 18 to 24, all of the rejected claims. Claims 25 and 26 have been indicated to be allowable. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF INVENTION

The invention relates to a method of fabricating an SOI structure which includes the steps of providing a substrate having at least one of active or passive elements on a surface thereof (1 or 5) and providing a device wafer having at least one of active or passive elements on a surface thereof (5 or 1). An electrically insulating layer (3) is formed having a pair of opposed outer faces (not numbered), one of the opposed outer faces being disposed on a surface of one of the substrate or device wafer, the electrically insulating layer having an electrical interconnect structure (7, 9, 11) disposed therewithin, with a portion of the interconnect structure extending substantially to one of the outer faces of the electrically insulating structure to make electrical contact with a device in at least one of the device wafer and the substrate. The other of the outer faces of the electrically insulating layer is then bonded to the surface of the other of the substrate or device wafer. A voltage can be applied across a portion of the electrically insulating layer sufficient to break down the portion of the electrically insulating layer while maintaining the integrity of the remainder of the SOI structure to break down any electrically insulating region which may be interposed between the interconnect and a device in the substrate or device wafer. The interconnect path can be an extension of the device layer. The substrate is a semiconductor substrate or a semiconductor substrate and a dielectric.

ISSUES

The issues on appeal are as follows:

1. Whether claims 1, 3, 7 to 9, 18 to 21, 23 and 24 are anticipated by Hayashi (U.S. 5,087,585).

2. Whether claims 1 to 4, 7 to 9 and 18 to 24 are patentable over Hayashi in view of Applicant's Admitted Prior Art (AAPA).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

ISSUE 1

Claims 1 to 4, 7 to 9 and 18 to 24 were rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (U.S. 5,087,585). The rejection is without merit as will be demonstrated.

The invention herein resides broadly in the formation of one of a substrate or a device layer secured to a dielectric layer having interconnect and optional passive component structure disposed in the dielectric layer and extending through the dielectric layer to a surface of the dielectric layer. The substrate or device layer is then planarized along with the exposed surface of the dielectric layer and the exposed surface and the substrate or device layer are then bonded together after being aligned. There is no build-up of layer upon layer as is found in Hayashi. Furthermore, the interconnect structure is disposed within the dielectric layer. No such arrangement is found in Hayashi. Still further, any insulation buildup between the interconnect and the device in the substrate to which interconnection is to be made is obviated by the

application of a sufficiently high voltage across the insulation buildup, when necessary, between the interconnect and the device in the substrate to break down the intervening insulation and provide contact between the interconnect and the device in the substrate of device layer. It follows that the structures of Hayashi and the subject invention and the method of fabrication of the two are entirely different and unrelated to each other.

More specifically, and with reference to claim 1, this claim requires, among other steps, forming an electrically insulating layer having a pair of opposed outer faces, one of the outer faces disposed on the surface one of the substrate or the device wafer, the electrically insulating layer having an electrical interconnect structure disposed therewithin. No such step is taught or suggested by Hayashi either alone or in the combination as claimed. The insulative layer of Hayashi has no such arrangement. There is no interconnect in Hayashi and, in the event the non-refractory metal pool 18 is alleged to be such interconnect, which it is not, this element is not disposed within the insulative layer 17. It follows that this element is not found in Hayashi either as presently or previously claimed.

Claim 1 further requires that a portion of the interconnect structure extend substantially to the one of the outer faces of the electrically insulating structure to make electrical contact with a device in at least one of the device wafer and the substrate. No such arrangement is found in Hayashi either alone or in the combination as claimed. The pool 18 of Hayashi is not disposed at a surface of the electrically insulating structure and is not shown as being connected to anything in the second layer thin film device 23 other than the layer itself.

Claim 1 yet further requires the step of <u>then</u> bonding the other of the outer faces of the electrically insulating layer to the surface of the other of the substrate or device wafer. No such

step is taught or suggested by Hayashi either alone or in the combination as claimed. The order of the steps is specifically claimed and this order is nowhere taught or suggested by Hayashi.

Claims 2 to 4 depend from claim 1 and therefore define patentably over Hayashi for at least the reasons presented above with reference to claim 1.

Claim 2 further limits claim 1 by requiring the step of applying a voltage across a portion of the electrically insulating layer sufficient to break down the portion of the electrically insulating layer while maintaining the integrity of the remainder of SOI structure. No such combination is taught or suggested by Hayashi.

Claim 3 further limits claim 1 by requiring that at least one of the device layer and the substrate include a bond region, the interconnect structure contacting the bond region. insulating layer sufficient to break down said portion of said electrically insulating layer while maintaining the integrity of the remainder of said SOI structure. No such combination is taught or suggested by Hayashi.

Claim 4 further limits claim 2 by requiring that at least one of the device layer and the substrate include a bond region, the interconnect structure contacting the bond region through the portion of the electrically insulating layer. No such combination is taught or suggested by Hayashi.

Claim 7 requires, among other steps, provision of an SOI structure having a device layer having at least one of active or passive elements on a surface thereof, a substrate having at least one of active or passive elements on a surface thereof and an electrically insulating layer having an interconnect structure disposed within the electrically insulating layer and extending to a surface of the electrically insulating layer. No such step is taught or suggested by Hayashi either alone or in the combination as claimed as discussed above with reference to claim 1.

Claim 7 further requires the steps of forming a substantially planar region on the surface of the device layer and the surface of the substrate and a region on the surface of the electrically insulating layer, interposing the electrically insulating layer between the device layer and the substrate with the planar region of the electrically insulating layer overlaying the substantially planar region on the at least one of the surface of the device layer and the surface of the substrate to make electrical contact with a device in at least one of the device wafer and the substrate and then bonding the surface to the other of the substrate wafer and device layer. No such steps are taught or suggested by Hayashi either alone or in the combination as claimed. Note the argument presented in connection with claim 1 as well as the fact that Hayashi has no electrically insulating layer having an interconnect structure which provides the claimed interconnect function in the electrically insulating layer bonded to one of the device layer or substrate after being affixed to the other of these elements in the manner claimed.

Claims 8 and 9 depend from claim 7 and therefore define patentably over Hayashi for at least the reasons presented above with reference to claim 7.

In addition, claim 8 further limits claim 7 by requiring the step of forming an electrical interconnect structure in the electrically insulating layer, the interconnect structure contacting at least one of the device layer and the substrate. No such step is taught or suggested by Hayashi either alone or in the combination as claimed. The interconnect structure of Hayashi is not "in the electrically insulating layer" but rather is external thereto.

Claim 9 further limits claim 7 by requiring the step of forming an electrical interconnect structure in the electrically insulating layer, the interconnect structure contacting both the device layer and the substrate. The argument applied as to claim 8 applies herein as well.

Claim 18 requires, among other steps, after providing a device layer having at least one of active or passive elements on a surface thereof and providing a substrate having at least one of active or passive elements on a surface thereof, providing a dielectric bonded to one of the device layer and the substrate having an interconnect disposed therein and extending to at least one surface thereof. No such step is taught or suggested by Hayashi either alone or in the combination as claimed.

Claim 18 further requires the step of then bonding the dielectric to the other of the device layer and the substrate to form an interface with the one of said device layer and the substrate and form an electrically conductive path across the interface to the interconnect. No such step or steps in the order claimed are taught or suggested by Hayashi.

Claims 19 to 24 depend from claim 18 and therefore define patentably over Hayashi for at least the reason presented above with reference to claim 18.

In addition, claim 19 further limits claim 18 by requiring that the electrically conductive path contacts the other of the device layer and the substrate. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claims 20 and 21 further limit claims 18 and 19 by requiring that the electrically conductive path be an extension of said device layer. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claim 22 further limits claim 18 by requiring that the step of forming an electrically conductive path across the interface to the interconnect be formed by breakdown of the dielectric. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof.

Claim 23 further limits claim 18 by requiring that the substrate be a semiconductor substrate. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claim 24 further limits claim 18 by requiring that the substrate comprise a semiconductor substrate and a dielectric. No such combination of steps in the order claimed is taught or suggested by Hayashi.

With reference to the statement by the Examiner that "Applicant's arguments is (sic) generally constructed as a restatement of each and every claim with *mere allegations* that Hayashi fails to teach or suggest said limitations/features" and that "Applicant has provided no substantive argument to support such allegations of absence of said features", the Examiner appears to have a misunderstanding as to what is being argued and what is his or her function. An argument directed to the specific wording of the claims could not be more specific. The argument specifically points that which is being claimed either alone and/or in combination, as the case may be, which is not taught or suggested by cited art, as the case may be. It is the duty of the Examiner to then either allow the claims or to reject the claims by making a prime facie case of non-patentability. It is not the duty of applicant to initially provide support for the absence of features as alleged in the final rejection. Rather, it is the duty of the Examiner to provide support for the allegation of the presence of features. This has not been done as is evident from the argument presented above and hereinbelow.

With reference to the Examiner being perplexed as to the position of appellant as to the interconnect 18 of Hayashi, this is a metal pool and is not at the surface of the interconnect to which reference is being made. The metal pool 18 of Hayashi is disposed in an aperture in the layer 17 and is otherwise unrelated to the layer 17 in any way. This structure does not read on that which is being claimed.

ISSUE 2

Claims 1 to 4, 7 to 9 and 18 to 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi in view of Applicant's admitted prior art. The rejection is without merit.

ALLOWABLE CLAIMS

Claims 25 and 26 depend from claims 1 and 7 respectively and have been indicated to be allowable if rewritten in independent form.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

1. A method of fabricating an SOI structure which comprises the steps of:

(a) providing a substrate having at least one of active or passive elements on a surface thereof;

(b) providing a device wafer having at least one of active or passive elements on a surface thereof;

(c) forming an electrically insulating layer having a pair of opposed outer faces, one of said opposed outer faces disposed on a said surface of one of said substrate or said device wafer, said electrically insulating layer having an electrical interconnect structure disposed therewithin, a portion of said interconnect structure extending substantially to said one of said outer faces of said electrically insulating structure to make electrical contact with a device in at least one of the device wafer and the substrate; and

(c) then bonding the other of said outer faces of said electrically insulating layer to the said surface of the other of said substrate or device wafer .

2. The method of claim 1 further including the step of applying a voltage across a portion of said electrically insulating layer sufficient to break down said portion of said electrically insulating layer while maintaining the integrity of the remainder of said SOI structure.

3. The method of claim 1 wherein at least one of said device layer and said substrate includes a bond region, said interconnect structure contacting said bond region.

4. The method of claim 2 wherein at least one of said device layer and said substrate includes a bond region, said interconnect structure contacting said bond region through said portion of said electrically insulating layer..

7. A method of forming an SOI structure, comprising the steps of:

providing a device layer having at least one of active or passive elements on a surface thereof;

providing a substrate having at least one of active or passive elements on a surface thereof;

providing an electrically insulating layer having an interconnect structure disposed therein and extending to a surface thereof;

forming a substantially planar region on said surface of said device layer and said surface of said substrate;

forming a substantially planar region on said surface of said electrically insulating layer;

interposing said electrically insulating layer between said device layer and said substrate with said planar region of said electrically insulating layer overlaying said substantially planar region on said at least one of said surface of said device layer and said surface of said substrate to make electrical contact with a device in at least one of the device wafer and the substrate; and

then bonding said planar surface of said electrically insulating layer to said overlying one of said substrate and said device layer.

8. The method of claim 7 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting at least one of said device layer and said substrate.

9. The method of claim 7 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting both said device layer and said substrate.

18. A method of fabricating an integrated circuit which comprises the steps of:

(a) providing a device layer having at least one of active or passive elements on a surface thereof;

(b) providing a substrate having at least one of active or passive elements on a surface thereof;

(c) providing a dielectric bonded to one of said device layer and said substrate having an interconnect disposed therein and extending to at least one surface thereof;

(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate and forming an electrically conductive path across said interface to said interconnect.

19. The method of claim 18 wherein said electrically conductive path contacts the other of said device layer and said substrate.

20. The method of claim 18 wherein said electrically conductive path is an extension of said device layer.

21. The method of claim 19 wherein said electrically conductive path is an extension of said device layer.

22. The method of claim 18, further including a dielectric disposed over said interconnect at said interface preventing electrical conduction across said interface, wherein said step of forming an electrically conductive path across said interface to said interconnect is formed by breakdown of said dielectric.

22. The method of claim 18 wherein said step of forming an electrically conductive path across said interface to said interconnect is formed by breakdown of said dielectric.

23. The method of claim 18 wherein said substrate is a semiconductor substrate.

24. The method of claim 18 wherein said substrate comprises a semiconductor substrate and a dielectric.

25. The method of claim 1 further including the steps of forming an electrical insulation on at least one of said electrically insulating layer, said substrate or said device wafer insulating said interconnect structure from said device in said at least one of the device wafer and the substrate and applying a voltage across said electrical insulation to break down said electrical insulation an provide interconnection between said interconnect structure and said device.

26. The method of claim 7 further including the steps of forming an electrical insulation on at least one of said electrically insulating layer, said substrate or said device wafer insulating said interconnect structure from said device in said at least one of the device wafer and the substrate and applying a voltage across said electrical insulation to break down said electrical insulation an provide interconnection between said interconnect structure and said device.